CLAIM LISTING

1. (Previously presented): An electrical device comprising:

first and second substrates having respective first and second integrated circuits, wherein at least one of the first substrate or the second substrate has a semiconductor layer thereon; and

a bond structure bonding the first substrate to the second substrate, the bond structure including an alloy:

bonded to the semiconductor layer;

composed of noble metal alloyed with an oxide affinity material having an affinity for oxygen higher than that of the material of which the semiconductor layer is composed such that the alloy is sufficient to remove a native oxide from an interface surface between the bond structure and the first substrate; and

configured to form an electrical connection between the first integrated circuit and the second integrated circuit.

2. (Original): The electrical device as defined in Claim 1, wherein the oxide affinity material is not more than about half the weight of the alloy interfacing the semiconductor layer.

3. (Original): The electrical device as defined in Claim 1, further comprising electrical insulation, situated between the first and second

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substrates electrical insulation, for electrically isolating a plurality integrated circuits.

4. (Original): The electrical device as defined in Claim 1, further comprising a region having a closed environment between the first and second substrates, wherein the region is defined at least in part by the bond structure.

5. (Cancelled).

6. (Original): The electrical device as defined in Claim 1, wherein the alloy bonded to the semiconductor layer is sufficient to maintain an alignment of said first substrate with respect to the second substrate.

7. (Original): The electrical device as defined in Claim 1, wherein the alloy bonded to the semiconductor layer is composed of noble metal alloyed with an oxide affinity material having a free energy that is lower than that of silicon dioxide.

8. (Original): The electrical device as defined in Claim 1, wherein the alloy bonded to the semiconductor layer is composed of noble metal alloyed with a material having a free energy less than a range from about -200 Kcal/mol to about -205 Kcal/mol.

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9. (Original): The electrical device as defined in Claim 1, wherein the alloy bonded to the semiconductor layer is composed of noble metal alloyed with a material selected from the group consisting of Al, As, B, Ca, Ce, Co, Cr, Fe, Ga, Hf, In, La, Li, Mg, Mn, Nb, Nd, Ge, Pr, Sb, Si, Ta, Th, Ti, V, W, and Zr.

10. (Previously presented): An electrical device comprising first and second semiconductor wafers each including a plurality of integrated circuits, wherein:

the first semiconductor wafer has a silicon layer thereon;

the silicon layer on the first semiconductor wafer is bonded to the second semiconductor wafer by gold alloyed with an oxide affinity material having an oxygen affinity higher than that of silicon such that the gold alloyed with the oxide affinity material is sufficient to remove a native oxide from the first semiconductor wafer; and

the gold alloyed with the oxide affinity material is configured to provide an elcctrical connection between at least one said integrated circuit of the first semiconductor wafer with at least one said integrated circuit of the second semiconductor wafer.

11. (Original): The electrical device as defined in Claim 10, wherein the oxide affinity material makes up not more than about half the weight of the gold.

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12. (Cancelled).

13. (Cancelled).

14. (Original): The electrical device as defined in Claim 10, further comprising a hermetically sealed region between the first and second semiconductor wafers that is defined in part by:

the silicon layer on the first semiconductor wafer; and

the gold alloyed with the oxide affinity material.

15. (Previously presented): An electrical device comprising:

first and second semiconductor wafers each including a plurality of integrated circuits;

silicon on the first semiconductor wafer; and

a bonding structure including gold alloyed with a material having a free energy lower than that of silicon dioxide, wherein the first semiconductor wafer is bonded to the second semiconductor wafer by the gold alloy that is bonded to the silicon on the first semiconductor wafer such that the gold alloy is configured to:

remove a native oxide from the silicon; and

provide an electrical connection between at least one said integrated circuit of the first semiconductor wafer with at least one said integrated circuit of the second semiconductor wafer.

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16. (Original): The electrical device as defined in Claim 15, wherein the free energy of the material is less than a range from about -200 Kcal/mol to about -205 Kcal/mol.

17. (Original): The electrical device as defined in Claim 15, wherein the material selected from the group consisting of Ti Al, Li, Mg, and Ca.

Claims 18-32 (Cancelled).

33. (Previously presented): An electrical device comprising first and second substrates bonded together with a first material having dispersed therein a reducing agent for the diffusion therein of oxidation of a second material of which at least one of the first and second substrates is composed, wherein:

the reducing agent has a higher affinity for oxygen than that of the second material; and

the first material having the dispersed reducing agent is configured to:

remove a native oxide from the first substrate or the second substrate; and

form an electrical connection between a first integrated circuit on the first substrate with a second integrated circuit on the second substrate.

34. (Original): The electrical device as defined in Claim 33, wherein:

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the first material comprises gold; and

the second material comprises silicon.

Claims 35-59 (Cancelled).

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